

# Serial server

Using the serial server, access to different serial interfaces is possible via a TCP/IP-connection.

In version 1.4, the following interfaces are supported:

- Asynchronous serial interace full-duplex - UART
- Synchronous serial interface full-duplex - SPI Master
- TCP/IP - modem at synchronous serial interface half-duplex - SPI Slave
- Two-Wire interface- I2C Master

Netzwerkname:  .local

HTTP Port:

GPIO TCP Port:   Aktiv

Serieller Modus:

Serieller Port:

Änderungen werden erst nach ...

The interface as well as the TCP/IP-port of the serial server are set on the website with the general settings. The new settings always become only active after restart of the Netzer.

The interfaces occupy different [IOs](#) of the Netzer. A free configuration of those is then not possible from the [GPIO-main page](#).

Apart from the TCP/IP-modem, all modes are structures that way that after restart Netzer opens a socket with a correspondingly configured port and listens to incoming connections.

Once a connection is made, it is then possible to directly send data to the respective serial interface and received by it as well. Depending on the chosen interface, a certain protocol overhead is still required to be transferred.

A receive buffer and a send buffer are interposed between the TCP/IP-socket. Both buffers have 256 byte. All data communication is done via these buffers to increase the data throughput on the serial interfaces.

## Settings

**STATUS**

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**ALLGEMEIN**

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**GPIO**

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**• SERIELL**

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UART Einstellungen

UART Baudrate:

Allgemeine SPI Einstellungen (SPI Slave: Änderungen erst nach Neustart)

Taktmodus:
 

- SPI Mode 0
- SPI Mode 1
- SPI Mode 2
- SPI Mode 3

SPI Master Einstellungen

Taktfrequenz:

Abtastung des Eingangs:
 

- In der Mitte
- Am Ende

I2C Master Einstellungen (SCL = SPI\_CLK, SDA = SPI\_MI)

Taktfrequenz:

## SPI

For SPI, particularly the clock mode is important. The setting applies likewise to Master and Slave. It defines the polarity of the clock signal as well as the transfer edge as follows:

Mode	Idle mode of the clock signal	transfer edge
Mode 0	0	rising
Mode 1	0	falling
Mode 2	1	falling
Mode 3	1	rising



For the successful data transfer, the modes of Master and Slave should be equivalent!

Amendments of this setting at the SPI-slave become effective after restart only.



In SPI-slave mode it is important that the Master actually creates the set resting potential for the clock signal at the beginning, since otherwise the Netzer may not activate the SPI-module!

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